EXHIBIT A

I hereby certify that this correspondence is being filed via EFS-Web with the United States Patent and Trademark Office on October 7, 2013.

KILPATRICK TOWNSEND & STOCKTON LLP

By: /Kelly Mak/

PATENT
Attorney Docket No.: 90523-003710US-789306
Client Ref. No.: ECC-0407-US-2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Sameep Dave et al.

Application No.: 12/858,510

Filed: August 18, 2010

For: FORWARD ERROR CORRECTION WITH PARALLEL ERROR DETECTION FOR FLASH MEMORIES

Customer No.: 61668

Confirmation No.: 6028

Examiner: Elmira Mehrmanesh

Technology Center/Art Unit: 2113

AMENDMENT AFTER ALLOWANCE UNDER 37 CFR § 1.312

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Commissioner:

In response to the Notice of Allowance mailed August 20, 2013, please enter the following amendments and remarks:

Amendments to the Specification begin on page 2 of this paper.

Remarks/Arguments begin on page 3 of this paper.

REMARKS/ARGUMENTS

This Amendment is in response to the Notice of Allowance mailed August 20, 2013 (hereinafter "Notice of Allowance"). The pending claims 1-25 are allowed and are not amended herein.

In response to the Non-Final Office Action mailed January 31, 2013, Applicants submitted an amendment to the title of the Specification in the Response filed April 29, 2013. On page 2 of the Notice of Allowability included with the Notice of Allowance, the Examiner acknowledged Applicants' amendment to the title and withdrew the objection to the Specification. However, the first page of the Notice of Allowance does not reflect the amended title.

Accordingly, Applicants are resubmitting the amendment to the title of the Specification along with a Supplemental Application Data Sheet to update the record with the amended title, as approved by the Examiner. Correction of the title is respectfully requested.

CONCLUSION

Entry of this amendment is respectfully urged since no additional search is required, no more than a cursory review of the record is needed, and the amendments do not require a substantial amount of work on the part of the Office.

If the Examiner believes a telephone conference would expedite prosecution of this application, please contact the undersigned at (650) 326-2400.

Respectfully submitted,

/Mymy N. Henderson/
Mymy N. Henderson
Registration No. 64,975

KILPATRICK TOWNSEND & STOCKTON, LLP

Attachment

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Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

1. (Currently Amended) A flash memory decoder comprising:

a decoding module configured to:

receive encoded data from the flash memory; and

decode the received encoded data to generate a plurality of partially decoded data streams;

an error detection module communicatively coupled with the decoding module, and comprising a plurality of error detection sub-modules operating in parallel, each error detection sub-module configured to:

receive a different one of the plurality of partially decoded data streams;

detect whether a portion of the respective received stream contains an error; and

forward the portion of the respective received stream containing an error to an error correction module; and

[[an]] the error correction module, communicatively coupled with and physically separate from the error detection module, and configured to correct the received portions of the respective received streams containing an error.

2. (Currently Amended) The flash memory decoder of claim 1, wherein each of the error detection sub-modules is configured to read data from a set of one or more sectors of flash memory different from other of the error detection sub-modules.

3. (Original) The flash memory decoder of claim 2, further comprising a read controller configured to dynamically modify the error detection sub-modules assigned to at least a subset of the sectors of flash memory.

4. (Original) The flash memory decoder of claim 1, wherein the error correction module comprises a plurality of error correction sub-modules operating in parallel and fewer in number than the error detection sub-modules.

5. (Original) The flash memory decoder of claim 4, further comprising a power controller configured to selectively power-up one or more of the error correction sub-modules responsive to an age of the flash memory.

6. (Currently Amended) The flash memory decoder of claim 4, further comprising:

an error monitoring module, communicatively coupled with the error detection module, and configured to monitor a rate of errors from the error detection module,

wherein [[the]] a power controller is configured to selectively power-up one or more of the error correction sub-modules when the monitored rate of errors exceeds a threshold.

7. (Original) The flash memory decoder of claim 4, further comprising:

an error monitoring module, communicatively coupled with the error detection module, and configured to monitor a rate of errors from the error detection module for each of a plurality of sectors of the flash memory,

wherein a power controller is configured to selectively power-up an error correction sub-module for assignment to a set of one or more of the monitored sectors when the monitored rate of errors for the set exceeds a threshold.

8. (Original) The flash memory decoder of claim 4, wherein,

each error correction sub-module is assigned a set of two or more error detection sub-modules different from error detection sub-modules associated with other of the error correction sub-modules; and

each error correction sub-module is configured to receive portions of the respective received streams containing an error detected in parallel by the set of two or more error detection sub-modules assigned to the respective error correction sub-module.

9. (Original) The flash memory decoder of claim 1, further comprising a read controller configured to selectively power-down one or more subsets of the error detection sub-modules.

10. (Original) The flash memory decoder of claim 1, further comprising:

the flash memory, communicatively coupled with the decoding module;

an encoder, communicatively coupled with the flash memory, and configured to encode data at a coding rate for storage as the encoded data on the flash memory; and

an adaptive encoding rate controller configured to modify the coding rate responsive to an age of the flash memory.

11. (Original) The flash memory decoder of claim 1, further comprising:

an error monitoring module, communicatively coupled with the error detection module, and configured to monitor a rate of errors from the error detection module; and

an adaptive encoding rate controller configured to modify a coding rate for a flash memory encoding module when the monitored rate of errors exceeds a threshold.

12. (Original) The flash memory decoder of claim 1, further comprising:

an error monitoring module, communicatively coupled with the error detection module, and configured to monitor a rate of errors from the error detection module for each of a plurality of sectors of the flash memory; and

an adaptive encoding rate controller configured to modify a coding rate of a set of one or more of the monitored sectors when the monitored rate of errors for the set exceeds a threshold.

13. (Original) The flash memory decoder of claim 1, wherein each error detection sub-module is configured to direct error-free portions of the respective received streams to bypass the error correction module.

14. (Original) The flash memory decoder of claim 1, wherein,

the error detection module comprises the decoding module; and

the encoded data is encoded with a Hamming code, a BCH code, a Turbo code, or a low-density parity check code.

15. (Original) A system comprising:

an encoder configured to encode data for storage on a flash memory;

the flash memory, communicatively coupled with the encoding module, and configured to store the encoded data; and

a decoder, communicatively coupled with the flash memory, and configured to:

retrieve the encoded data from flash memory to generate a plurality of data streams; and

process, at each of a plurality of error detection sub-modules of the decoder operating in parallel, a different one of the plurality of data streams, wherein each error detection sub-module is configured to:

detect whether a portion of the respective received stream contains an error; and

forward the portion of the respective received stream containing an error to an error correction module of the decoder; and

correct, with the error correction module physically separate from the error detection module, the forwarded portions of the respective received streams containing an error.

16. (Original) The system of claim 15, wherein the encoder is further configured to adaptively modify the coding rate responsive to an age of the flash memory or a rate of errors associated with the decoded data.

17. (Original) A method comprising:

receiving encoded data from a flash memory comprising a plurality of data streams;

processing, at each of a plurality of error detection sub-modules operating in parallel, a different one of the plurality of data streams, wherein each error detection sub-module is configured to:

detect whether a portion of the respective received stream contains an error; and

forward the portion of the respective received stream containing an error to an error correction module; and

correcting, with the error correction module physically separate from an error detection module, the forwarded portions of the respective received streams containing an error.

18. (Original) The method of claim 17, further comprising:

dynamically modifying the error detection sub-modules assigned to receive data from respective sectors of flash memory.

19. (Original) The method of claim 17, wherein the error correction module comprises a plurality of error correction sub-modules operating in parallel and fewer in number than the error detection sub-modules.

20. (Original) The method of claim 19, further comprising:

powering-up, from an inactive mode, one or more of the error correction sub-modules responsive to an age of the flash memory.

21. (Original) The method of claim 19, further comprising:

monitoring a rate of errors from the error detection module; and

powering-up one or more of the error correction sub-modules when the monitored rate of errors exceeds a threshold.

22. (Original) The method of claim 19, further comprising:

monitoring a rate of errors from the error detection module for each of a plurality of sectors of the flash memory; and

powering-up an error correction sub-module for assignment to a set of one or more of the monitored sectors when the monitored rate of errors for the set exceeds a threshold.

23. (Original) The method of claim 17, further comprising:

modifying a coding rate for data to be stored as the encoded data on the flash memory responsive to an age of the flash memory.

24. (Original) The method of claim 17, further comprising:

monitoring a rate of errors from the error detection module; and

modifying a coding rate for data to be stored as the encoded data on the flash memory when the monitored rate of errors exceeds a threshold.

25. (Currently Amended) The method of claim 17, further comprising:

monitoring a rate of errors from the error detection module for each of a plurality of sectors of the flash memory; and

modifying a coding rate for data to be stored as the encoded data on a set of one or more of the monitored sectors of the flash memory when the monitored rate of errors for the set exceeds a threshold.

REMARKS/ARGUMENTS

This Amendment is in response to the Office Action mailed January 31, 2013 ("Office Action"). Claims 1-25 were pending in the present application. This Amendment amends claims 1-2, 6, and 25 to correct clerical errors. Claims 1-25 remain pending in the application. Applicants submit that no new matter has been introduced by virtue of these amendments. Reconsideration of the rejected claims is respectfully requested.

THE SPECIFICATION

The title of the invention is allegedly not descriptive. Applicants have amended the title.

THE CLAIMS

Allowable Subject Matter

Applicants appreciate the indication of allowability of claims 3-12, 16, and 18-25 if rewritten in independent form to include the limitations of their respective base claims. As discussed below, the independent claims 1, 15, and 17 are allowable over the cited reference; hence, claims 3-12, 16, and 18-25 are each patentable at least for the reason of depending from a respective allowable claim.

35 U.S.C. § 102 Rejection of Claims 1, 2, 13-15 and 17

Claims 1-2, 13-15, and 17 are rejected under 35 U.S.C. §102(b) as allegedly being anticipated by U.S. Patent Publication No. 2005/0138521 to Suzuki et al. (hereinafter "Suzuki").

Claims 1, 15, and 17

Claim 1 recites a flash memory decoder comprising a decoding module, an error detection module, and an error correction module. The decoding module is configured to decode received encoded data to generate a plurality of partially decoded data streams. The error detection module comprises a plurality of error detection sub-modules operating in parallel, where each error detection sub-module is configured to receive a different one of the partially decoded data streams, and to detect whether a portion of the respective received stream contains an error. The error correction module, which is physically separate from the error detection

module, is configured to correct received portions of the respective received streams containing an error. Applicants submit that at least some of these elements are not disclosed in Suzuki.

Suzuki is directed to a forward error correction (FEC) decoder that extracts FEC parameters encoded into a signal stream to adaptively change operational parameters. See Abstract. Suzuki's receiver includes an FEC chain decoding functional block and a parameter extraction functional block. See para. [0016]. The FEC chain decoding functional block decodes FEC blocks and detects if an FEC block is a Control Packet (CP) that includes FEC parameters. See Abstract, para. [0016]. The FEC chain decoding functional block is configured for the CP format, and all FEC blocks are decoded as being CPs, such that an error will be detected and flagged, by setting an error flag high, if the FEC block is not a CP. See para. [0140]-[0142]; FIG. 18B. If the error flag is set low (indicating an actual CP is detected/decoded), the parameter extraction functional block then processes the CP to extract the FEC parameters from the CP. See para. [0022] and [0140]-[0142]; FIG. 18B. The extracted FEC parameters are later used by the FEC chain decoding functional block for decoding subsequent FEC blocks. See para. [0017].

The Office Action relies on Suzuki at paragraphs [0122]-[0123] for the feature of the decoding module being configured to decode received encoded data to generate a plurality of partially decoded data streams. Paragraphs [0122]-[0123] of Suzuki refer to FIG. 13, which illustrates the functionality of the FEC decoding chain (i.e., the FEC chain decoding functional block). The FEC decoding chain of FIG. 13 includes, in series, a turbo decoder, a de-interleaver, a Reed Solomon (RS) decoder, a descrambler, and an MPEG packetizer. Paragraphs [0122]-[0123] describe a demodulator receiving an input signal and generating a Queue Block (QB) stream including Turbo Blocks (TBs). However, the cited paragraphs of Suzuki only discuss demodulating a single stream of data – the QB stream. This single QB stream is processed serially by the functional blocks of the FEC decoding chain of FIG. 13. In contrast, the claimed decoding module is configured to decode received encoded data to generate a plurality of partially decoded data streams. Thus, not only does the cited portion disclose demodulating versus the claimed decoding, only a single stream is disclosed versus the claimed plurality of streams. Accordingly, at least this feature of claim 1 is not shown in Suzuki.

Moreover, the claimed error detection module is also not disclosed in Suzuki. The claimed error detection module comprises a plurality of error detection sub-modules

operating in parallel, where each error detection sub-module is configured to receive a different one of the partially decoded data streams, and to detect whether a portion of the respective received stream contains an error. Thus, the multiple error detection sub-modules perform the same function on different streams. For the claimed error detection module and its functions, the Office Action relies on paragraphs [0123] and [0022] of Suzuki. As discussed above, paragraph [0123] describes the demodulator demodulating the single QB stream. Paragraph [0022] discusses the FEC decoding chain using an error flag when decoding/detecting a CP (Control Packet), and in response to the error flag setting, the CP processor extracting FEC parameters from the CP. However, the cited portions of Suzuki fail to disclose the claimed error detection module. The claimed error detection module comprises a plurality of error detection sub-modules performing the same functions and operating in parallel, whereas in Suzuki, the various functional blocks (e.g., the demodulator, blocks of the FEC decoding chain, the CP processor) perform different functions and operate serially. Accordingly, the features of the error detection module are also not shown in Suzuki.

Furthermore, the claimed error correction module is also not disclosed in Suzuki. The claimed error correction module, which is physically separate from the error detection module, is configured to correct received portions of the respective received streams containing an error. For the claimed error correction module, the Office Action relies on paragraph [0142] of Suzuki. As discussed above, paragraph [0142], which refers to FIG. 18B, describes the FEC chain decoding functional block decoding all FEC blocks as being CP, such that if an FEC block is not a CP, an error will be detected and flagged by setting the error flag high. If the FEC block is an actual CP, the error flag will be set low. A low error flag directs the CP processor (i.e., the parameter extraction functional block) to extract the FEC parameters from the CP. However, the cited portions of Suzuki fail to disclose the claimed error correction module. The error correction module is configured to correct received portions of the respective received streams containing an error, whereas in Suzuki, an error (indicated by the error flag set high) is not actually corrected by the CP processor, but simply indicates that the CP processor should not attempt to extract FEC parameters from the non-CP FEC block. Moreover, the claimed error correction module is physically separate from the claimed error detection module, but the cited portions of Suzuki teach conventional turbo decoding and RS decoding, wherein error detection and error correction for the respective FEC code is not performed by modules which are

physically separate. Accordingly, these features of the error correction module are also not shown in Suzuki.

For the above reasons, at least these elements of claim 1 are not disclosed by the relied-upon portions of Suzuki. Therefore, claim 1 is patentable over Suzuki. Applicants respectfully request withdrawal of the rejection and allowance of claim 1.

Claims 15 and 17 recite features similar to those discussed above with reference to claim 1. The Office Action rejected claims 15 and 17 under similar rationales as applied against claim 1. For at least similar reasons as those stated with respect to claim 1, claims 15 and 17 are patentable over Suzuki. Applicants respectfully request withdrawal of the rejections and allowance of claims 15 and 17.

Claims 2 and 13-14

Claims 2 and 13-14 depend from and incorporate all the features of independent claim 1. For at least the reasons stated above with respect to claim 1, claims 2 and 13-14 are patentable over Suzuki. Particular claims might have other reasons for allowability over the cited references, and not all of those reasons need be provided here. Applicants respectfully request withdrawal of the rejections and allowance of claims 2 and 13-14.

Amendments to the Claims

Unless otherwise specified, amendments to the claims are made for purposes of clarity, and are not intended to alter the scope of the claims or limit any equivalents thereof. The amendments are supported by the Specification as filed and do not add new matter.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

Further, the Commissioner is hereby authorized to charge any additional fees or credit any overpayment in connection with this paper to Deposit Account No. 20-1430.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,

/Mymy N. Henderson/
Mymy N. Henderson
Registration No. 64,975

KILPATRICK TOWNSEND & STOCKTON LLP
Two Embarcadero Center, Eighth Floor
San Francisco, California 94111-3834
Tel: 650-326-2400
Fax: 415-576-0300

Substitute for form 1449/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				**Application Number**	12/858,510
				Filing Date	August 18, 2010
				First Named Inventor	Dave, Sameep
				Art Unit	2117
(Use as many sheets as necessary)				Examiner Name	Gaffin, Jeffrey A.
Sheet	1	of	1	Attorney Docket Number	90523-789306 (003710US)

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1	US-2003-037299 A1	02-20-2003	Smith, Kenneth Kay	
	2	US-2004-243906 A1	12-2-2004	Huang, Che-Chi	
	3	US-2005-172179 A1	08-04-2005	Brandenberger, Sarah H.	
	4	US-2008-052564 A1	02-28-2008	Yim, Yong-Tae	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]	Number[4]	Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
	5	EP	1 612 950	A1	01-04-2006	St. Microelectronics SRL		☐
	6	EP	2 299 362	A2	05-04-2001	ViaSat, Inc.		☐
	7	WO	2006/013529	A1	02-09-2006	Koninkl Philpps Electronics NV		☐

NON PATENT LITERATURE DOCUMENTS

Examiner Initials *	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[6]
	8	European Search Report and Search Opinion of April 5, 2011 for European Application No. EP 2299362.	☐

Examiner Signature		Date Considered	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 3

Complete if Known	
Application Number	12/858,510
Filing Date	August 18, 2010
First Named Inventor	Dave, Sameep
Art Unit	
Examiner Name	
Attorney Docket Number	026258-003710US

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	AA	US-7,203,874	04-10-2007	Roohparvar	
	AB	US-7,296,213	11-13-2007	Vainsencher et al.	
	AC	US-7,394,689	07-01-2008	Ryu	
	AD	US-7,356,755	04-08-2008	Fackenthal	
	AE	US-6,751,766	06-15-2004	Guterman et al.	
	AF	US-2007/0204206	08-30-2007	Lee et al.	
	AG	US-2004/0083334	04-29-2004	Chang et al.	
	AH	US-2008/0244362	10-02-2008	Liu et al.	
	AI	US-2008/0072120	03-20-2008	Radke	
	AJ	US-2007/0266295	11-15-2007	Conley	
	AK	US-2008/0244370	10-02-2008	Lam	
	AL	US-2008/0163028	07-03-2008	Mokhlesi	
	AM	US-2007/0283428	12-06-2007	Ma et al.	
	AN	US-7,231,585	06-12-2007	Vainsencher et al.	
	AO	US-7,333,364	02-19-2008	Yu et al.	
	AP	US-2008/0148132	06-19-2008	Mavila	
	AQ	US-2003/0041299	02-27-2003	Kanazawa et al.	
	AR	US-2008/0270680	10-30-2008	Chang	
	AS	US-2007/0271494	11-22-2007	Gorobets	
	AT	US-2008/0130341	06-05-2008	Shalvi etal.	
	AU	US-2008/0184094	07-31-2008	Murray et al.	
	AV	US-2007/0266296	11-15-2007	Conley	
	AW	US-2006/0059406	03-16-2006	Micheloni et al.	
	AX	US-7,360,136	04-15-2008	Guterman et al.	
	AY	US-2007/0223277	09-27-2007	Tanaka et al.	
	AZ	US-7,304,893	12-04-2007	Hemink	
	BA	US-2008/0212371	09-04-2008	Roohparvar	
	BB	US-6,684,353	01-27-2004	Parker et al.	
	BC	US-2007/0171730	07-26-2007	Ramamoorthy et al.	
	BD	US-2008/0282128	11-13-2008	Lee et al.	
	BE	US-7,305,596	12-04-2007	Noda et al.	
	BF	US-2008/0109703	05-08-2008	Brandman	
	BG	US-2008/0168320	07-10-2008	Cassuto et al.	
	BH	US-2008/0276150	11-06-2008	Kong et al.	
	BI	US-2008/0301526	12-04-2008	Kohler et al.	

Examiner Signature		Date Considered	

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	BJ	US-2008/0313493	12-18-2008	Roohparvar et al.	
	BK	US-2009/0013234	01-08-2009	Radke	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] Number[4] Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
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						☐
						☐

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(Use as many sheets as necessary)				Examiner Name	
Sheet	3	of	3	Attorney Docket Number	026258-003710US

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	BA	STMicroelectronics, "Error Correction Code in NAND Flash Memories", http://www.eetasia.com/ARTICLES/2004NOV29 MEM_AN10.PDF?SOURCES=DOWNLOAD, May 11, 2004.	☐
	BB	Numonyx, "Error Correction Code in Single Level Cell NAND Flash Memories", http://www.numonyx.com/Documents/Application%20Notes/AN1823.pdf, May 26, 2008.	☐
	BC	Micron Technology, Inc., "ECC Module for Xilinx Spartan-3", http://download.micron.com/pdf/technotes/nand/tn2905.pdf, May 1, 2007.	☐
	BD	Micron Technology, Inc., "Hamming Codes for NAND Flash Memory Devices", http://download.micron.com/pdf/technotes/nand/tn2908.pdf, May 1, 2007.	☐
	BE	Sun et al., "Multilevel Flash Memory On-Chip Error Correction Based on Trellis Coded Modulation", http://www.ecse.rpi.edu/homepages/tzhang/pub/FLASHISCAS06.pdf.	☐
	BF	Micron Technology, Inc., "NAND Flash Design and Use Considerations", http://download.micron.com/pdf/technotes/nand/tn2917.pdf, August 1, 2006.	☐
	BG	Micron Technology, Inc., "Using COPYBACK Operations in NAND Flash Devices," http://download.micron.com/pdf/technotes/nand/tn2941_idm_copyback.pdf, October 1, 2008.	☐
	BH	Micron Technology, Inc., "NAND Flash Internal Data Move", http://download.micron.com/pdf/technotes/nand/tn2915.pdf, June 1, 2007.	☐
	BI	Micron Technology, Inc., "Wear-Leveling Techniques in NAND Flash Devices", http://download.micron.com/pdf/technotes/nand/tn2942_nand_wear_leveling.pdf, October 1, 2008.	☐
	BJ	Chen, et al., "Error Correction for Multi-Level NAND Flash Memory Using Reed-Solomon Codes", http://www.csie.ntu.edu.tw/~f95070/Flash%20Paper%20Collection/ERROR%20CORRECTION%20FOR%20MULTI-LEVEL%20NAND%20FLASH%20MEMORY%20USING%20REED-SOLOMON%20CODES.pdf, November 26, 2008.	

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.
[1] Applicant's unique citation designation number (optional). [2] Applicant is to place a check mark here if English language Translation is attached.

FORWARD ERROR CORRECTION FOR MEMORIES

CROSS-REFERENCES TO RELATED APPLICATIONS

[0001] This application claims priority from co-pending U.S. Provisional Patent Application No. 61/234,911, filed August 18, 2009, entitled "FORWARD ERROR CORRECTION FOR FLASH MEMORIES" (Attorney Docket No. 026258-003700US), which is hereby incorporated by reference, as if set forth in full in this document, for all purposes.

BACKGROUND

[0002] The present invention relates to forward error correction (FEC) in general and, in particular, to FEC for flash memory. The advancements of flash memory technology in recent years has dramatically increased storage capacity and decreased the cost of non-volatile semiconductor memory. This has made Solid State Drives (SSDs) (typically a flash memory-based non-volatile memory system) an emerging substitute for magnetic Hard Disk Drive (HDD).

[0003] The use of FEC to enhance the reliability and longevity of flash memory is one of the challenges for making SSDs perform on par with HDDs.

SUMMARY

[0004] Methods, systems, and devices are described for forward error correction for flash memory. Encoded data from flash memory may be retrieved to generate a number of data streams (which may, but need not be, partially decoded). At each of a number of error detection sub-modules operating in parallel, a different one of the data streams is processed. Each error detection sub-module may detect whether a portion of the respective received stream contains an error, and forward the portion of the respective stream containing an error to an error correction module. An error correction module, physically separate from the error detection sub-modules, may correct the forwarded portions of the respective streams.

[0005] The age and error rate associated with the flash memory may be monitored, and a coding rate may be dynamically adapted to account for these factors. The error rate may be monitored on a per-sector basis and, therefore, the coding rate may be adapted on a per-sector

(or per-set of sectors) basis. As the error rate increases in certain sets of sectors, additional error-correction sub-modules assigned to those sectors may be powered-up to handle the increased error rate. In one example, there are fewer error correction sub-modules than error detection sub-modules; each error correction sub-module may be time-shared by a number of error detection sub-modules. Also, it is worth noting that the associations between flash memory sectors, error detection sub-modules, and error correction sub-modules may be changed dynamically in response to age and error rates, as well.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] A further understanding of the nature and advantages of the present invention may be realized by reference to the following drawings. In the appended figures, similar components or features may have the same reference label. Further, various components of the same type may be distinguished by following the reference label by a dash and a second label that distinguishes among the similar components. If only the first reference label is used in the specification, the description is applicable to any one of the similar components having the same first reference label irrespective of the second reference label.

[0007] **FIG. 1** is a block diagram of a flash memory decoder system according to various embodiments of the invention.

[0008] **FIG. 2** is a block diagram of a flash memory decoder according to various embodiments of the invention.

[0009] **FIG. 3** is a block diagram of a flash memory decoder system illustrating error detection and correction sub-modules according to various embodiments of the invention.

[0010] **FIG. 4** is a block diagram of a flash memory decoder system illustrating an architecture for a decoder controller according to various embodiments of the invention.

[0011] **FIG. 5** is a flowchart illustrating a method of decoding data from a flash memory according to various embodiments of the invention.

[0012] **FIG. 6** is a flowchart illustrating a method of age responsive decoding of data from a flash memory according to various embodiments of the invention.

[0013] **FIG. 7** is a flowchart illustrating a method of decoding data from a flash memory responsive to error rate according to various embodiments of the invention.

DETAILED DESCRIPTION

[0014] Methods, systems, and devices are described for forward error correction for flash memory. Encoded data from flash memory may be processed to generate a number of data streams. At each of a number of error detection sub-modules operating in parallel, a different one of the data streams is processed. Each error detection sub-module may detect whether a portion of the respective received stream contains an error, and forward the portion to an error correction module. An error correction module, physically separate from the error detection sub-modules, may correct the forwarded portions. The age and error rate associated with the flash memory may be monitored, and a coding rate or other aspects may be dynamically adapted to account for these factors.

[0015] This description provides example embodiments only, and is not intended to limit the scope, applicability, or configuration of the invention. Rather, the ensuing description of the embodiments will provide those skilled in the art with an enabling description for implementing embodiments of the invention. Various changes may be made in the function and arrangement of elements without departing from the spirit and scope of the invention.

[0016] Thus, various embodiments may omit, substitute, or add various procedures or components as appropriate. For instance, it should be appreciated that in alternative embodiments the methods may be performed in an order different from that described, and that various steps may be added, omitted, or combined. Also, features described with respect to certain embodiments may be combined in various other embodiments. Different aspects and elements of the embodiments may be combined in a similar manner.

[0017] It should also be appreciated that the following systems, methods, and software may individually or collectively be components of a larger system, wherein other procedures may take precedence over or otherwise modify their application. Also, a number of steps may be required before, after, or concurrently with the following embodiments.

[0018] Although much of the following discussion relates specifically to flash memory, aspects of the inventions are applicable to other forms of solid state memory. Generally, there are two predominant types of flash memory architectures: NOR and NAND. For the purposes of this disclosure, much discussion is directed to NAND-type flash, while again noting that principles set forth herein have wider applicability.

[0019] There are two primary NAND flash technologies. The earlier versions of NAND flash were Single-Level Cell (SLC). With SLC Flash, there is only one programmed state in addition to the erased state. The total of two states allows a single data bit to be stored in the

memory cell. The desire for higher density led to the more advanced Multiple-Level Cell (MLC). With MLC flash, there are multiple programmed states in addition to the erased state which allows multiple bits to be stored per memory cell.

[0020] Because of this increase in density and the related issues in manufacturing, one of the challenges for flash memory is to maintain high reliability and longevity. The deterioration of the oxide over time, and the disruptions from neighboring memory pages, can lead to data retention and corruption issues translating into bit errors. While the chances of any given data bit being corrupted is quite small, the vast number of data bits in a storage system makes the likelihood of data corruption a very real possibility. FEC may be one of the tools used to address these bit errors to improve the reliability and lifespan of flash memory.

[0021] Systems, devices, methods, and software are described for FEC for flash memory. Turning first to **FIG. 1**, a flash memory system 100 is illustrated. The system includes an encoder 105, flash memory 110, a decoder115, and a controller 120. This flash memory system 100 may be a stand-alone device, or may be integrated (in whole or in part) with a computer, server, phone or mobile device, tablet, television, or any other computing device.

[0022] Each of these system 100 components may be in communication with each other. The encoder 105, decoder 115, and controller 120 may, individually or collectively, be implemented with one or more Application Specific Integrated Circuits (ASICs) adapted to perform some or all of the applicable functions in hardware. Alternatively, the functions may be performed by one or more other processing units (or cores), on one or more integrated circuits. In other embodiments, other types of integrated circuits may be used (e.g., Structured/Platform ASICs, Field Programmable Gate Arrays (FPGAs), and other Semi-Custom ICs), which may be programmed in any manner known in the art. The functions of each unit may also be implemented, in whole or in part, with instructions embodied in a memory, formatted to be executed by one or more general or application-specific processors.

[0023] The encoder 105 may receive data to be stored, and encode the data (e.g., adding parity information) for storage in the flash memory 110 as encoded data. The decoder 115 may include a number of sub-components (not shown). An embodiment of the decoder 115 includes an error correction module in communication with and physically separate from an error detection module. The decoder 115 may process the encoded data to generate a number of data streams (which may, but need not be, decoded in whole or in part). The decoder 115 may process each stream at a different error detection sub-module operating in parallel in the

decoder 115. Each error detection sub-module may detect whether a portion of the respective received stream contains an error, and then forward the portion of the respective received stream containing an error to the error correction module. The error correction module may correct the forwarded portions of the respective received streams containing an error.

[0024] There are a number of different FEC schemes and codes that may be used in the flash memory system 100 introduced above. The system 100 functionality may be also be leveraged in a number of ways. For example, the error detection module may detect and flag bit errors, and this may allow sectors of memory with errors exceeding a threshold amount to be avoided by replacing such sectors with other sectors from a pool of available substitutes. The encoder 105 may, also or alternatively, change the code rate for the error-laden sections. As flash become more dense, the inherent bit error probability becomes higher.

[0025] Some simple FEC coding may be used to clean up these errors. The Hamming Code, with correction capacity of 1 bit and detection capability of 2, may be used with flash memory 110. With the desire for improving the performance, as well as the increased probability of inherent bit errors because of the denser memories, Bose Chaudhuri Hocqunghem (BCH) codes may be used, including the binary BCH and non-binary BCH (Reed Solomon (RS)) codes. These codes offer a higher correction capacity in comparison to the Hamming Code.

[0026] BCH encoding/decoding architectures may be the foundation of error correction in flash memory. However, there are more advanced coding options that may in some instances provide better performance than BCH codes. These codes may be used in flash memory 110, particularly for higher density flash and in applications where performance demands increase. Convolutional Turbo Codes (CTCs), Turbo Product Codes (TPCs), and low density parity check codes (LDPCs) are examples of the coding schemes that may be used. These state-of-the-art codes perform very close to the theoretical limits (Shannon Limits) of error correction, providing very high coding gain and improvement in Bit Error Rate (BER) performance for a given amount of redundancy.

[0027] Flash memory does have an inherent probability of error. Depending on the flash technology, this error rate may typically be somewhere between 1e-5 and 1e-8. To be able to match an HDD read/write bit error rate of 1e-15, a FEC scheme may be used**.** The measure of how good a job a code can perform in increasing the reliability depends upon its correction capacity. If the probability of bit error for flash memory 110 is p and the correction capacity

of the code is t bits over a codeword length of n bits, the probability of making an error may be expressed as:

$$p_{decoded} = \sum_{i=t+1}^{n} p^{i} \ *(1-p)^{n-i} \quad (1)$$

[0028] From equation (1), for a given p the higher the correction capacity of the code, the smaller the probability of error after the decoding will be. The correction capacity can be expressed as the number of bits a code can correct over a codeword length, or an input BER, or probability of error that it can take down to a certain target decoded BER. The advanced codes may correct more errors over a certain length, or take a higher input BER to create the same decoded BER.

[0029] There is incentive to use advanced codes for flash memory 110 even with not so dense memories. If the inherent error performance of flash memory 110 stayed at a certain low level, there would probably be decreased need for advanced codes. But, in practice, flash memory 110 performance tends to degrade over time. This means that even with an advanced code to help improve the reliability of a flash memory 110, over time the flash memory 110 may become lossy and, once the error rate is high enough, it may be beyond repair by the code being used.

[0030] In one example, the rate of errors or age of the flash memory 110 may be monitored, and the coding rate for data to be stored on the flash memory 110 may be modified in response thereto. Thus, a more robust coding rate may be used as the decoded error rate increases. The error monitoring may take place on a per-sector basis, and the code rate modification may similarly take place on a per-sector basis. In another example, the rate of errors or age of the flash memory 110 may be monitored, and error correction sub-modules may be powered-up in response thereto. Power savings may be achieved by keeping certain error correction sub-modules in an inactive mode until the flash memory reaches a certain age.

[0031] As noted, the flash memory 110 may be partitioned into a pool of small fixed-size sectors, and FEC may be applied on a sector-by-sector basis. The flash memory 110 size may be defined by the number of sectors that it contains. As there is a chance of sectors going bad over time, there may be a reserve/spare sector pool that allows the controller to replace the bad sectors by the spares as needed to extend the life of the flash. The error detection sub-module and error correction sub-modules may be dynamically assigned to various sectors, and the number powered-on may be increased or decreased.

[0032] A wear leveling technique may be used bb to make sure that various areas/sectors of the Flash "age" at a similar rate. Instead of the same sector being used over and over again, the read/writes are spread over much or the entire flash. And this translates into the probability of any sector being good (p_{good}) may be substantially the same for the various sectors in flash memory 110. If the size of the flash is N sectors and there are Δ spare sectors, the probability that the flash is still usable after time t is:

$$p_{usable} = \sum_{i=N}^{N+\Delta} (c_i^{N+\Delta} * (p_{good})^i * (1 - p_{good})^{N+\Delta-i}) \quad (2)$$

[0033] p_{good} may be a function of use time for the flash memory 110 sector. This is a component that is dependent upon the correction capacity of the code used. Thus, even with the spare sectors and the wear-leveling technique, the codes may play a key role in the flash being usable after a certain use time.

[0034] One of the concerns regarding advanced codes is how they fit into the sector sizes and overhead requirements of some flash memory architectures. TPC and LDPC codes offer an excellent degree of freedom in selecting the various code parameters like information block size, coded block size, and correction capacity, and would allow customization to suit any number of flash configurations.

[0035] **FIG. 2** is a block diagram 200 of a flash memory decoder 115-a according to various embodiments of the invention. The flash memory decoder 115-a may, for example, be the decoder 115 of FIG. 1, although flash memory decoder 115-a may be implemented in a number of other systems and devices, as well. The flash memory decoder 115-a includes a decoder module 205, an error detection module 210, and an error correction module 215, and each of may be in communication with each other. In one example, the error detection module 210 includes a number of sub-modules configured to detect errors on decoded streams of data. The error correction module 215 may be physically separate from each error detection sub-module, and may also include a number of sub-modules (each of which may be time-shared by a number of error detection sub-modules.

[0036] These components and sub-modules therein may, individually or collectively, be implemented with one or more Application Specific Integrated Circuits (ASICs) adapted to perform some or all of the applicable functions in hardware. Alternatively, the functions may be performed by one or more other processing units (or cores), on one or more integrated circuits. In other embodiments, other types of integrated circuits may be used (e.g., Structured/Platform ASICs, Field Programmable Gate Arrays (FPGAs), and other Semi-

Custom ICs), which may be programmed in any manner known in the art. The functions of each unit may also be implemented, in whole or in part, with instructions embodied in a memory, formatted to be executed by one or more general or application-specific processors.

[0037] The decoder module 205 may receive encoded data from flash memory, and process the received encoded data to generate a number of data streams. In one embodiment, the decoder module processor may buffer, de-interleave, or perform certain aspects of the decoding process, an thereby generate decoded (or partially decoded) data streams. As noted, the error detection module 210 may include a number of error detection sub-modules operating in parallel. Each (or a subset) of the error detection sub-modules may receive a different one of the data streams, and evaluate the respective stream to determine whether a portion of the stream contains an error. Each error detection sub-module may forward the portion of the respective received stream containing an error to the error correction module 215 (bypassing the error correction module 215 with the error-free portions). The error correction module 215 corrects the received portions of the respective received streams containing an error. As noted above, the error correction module 215 may include a number of sub-modules (each of which may be time-shared by a number of error detection sub-modules).

[0038] **FIG. 3** is a block diagram illustrating an example of an architecture for a flash memory decoder system 300 more particularly illustrating error detection and correction sub-modules. The flash memory decoder system 300 may, for example, be the system 100 of FIG. 1. The flash memory decoder system 300 includes flash memory 110-a, a decoder module 205-a, an error detection module 210-a, an error correction module 215-a, a controller 120-a, and an encoder 105-a. Each of these components may be in communication with each other.

[0039] The flash memory 110-a includes a number of different sets of one or more active sectors 305. The decoder module 205-a includes a number of decoder sub-modules 310, and each decoder sub-module 310 may be associated with a different set of sectors 305. The error detection module 210-a includes a number of error detection sub-modules 315, and each decoder sub-module 310 may be associated with a different set of sectors 305. Thus, encoded data may be read from a set of one or more of sectors 305 (e.g., sector(s) 305-a) by a decoder sub-module 310 (e.g., decoder sub-module 310-a), and processed (e.g., buffered, de-interleaved, decoded to some extent, etc.) to generate a data stream. The data stream may be forwarded to an error detection sub-module 315 (error detection sub-module 315-a). Thus, encoded data from a set of one or more of sectors 305-a may be sent to an error detection

sub-module 315-a. Different sets of sectors 305 may each send their respective data via different decoder sub-modules 310, as illustrated. In one embodiment, each error detection sub-module 315 is distinct from each other. In other embodiments, the decoder sub-module 310 and error detection sub-module 315 may be integrated to varying degrees.

[0040] Each error detection sub-module 315 may evaluate the respective stream to determine whether a portion of the stream contains an error. Each error detection sub-module 315 may forward the portion of the respective received stream containing an error to the error correction module 215-a (bypassing the error correction module 215 with the error-free portions). The error correction module 215-a includes a number of error correction sub-modules 320, each error correction sub-module 320 responsible for handling the errors from a number of error detection sub-modules 315 (e.g., error correction sub-module 320 may correct errors from error detection sub-modules 315-a, -b, and –c). Error correction sub-modules 320 may correct the received portions of the respective received streams containing an error. Each error correction sub-module 320 may receive portions of streams with errors, and these portion may have been detected in parallel.

[0041] Controller 120-a may perform a number of functions in the decoder process. Controller 120-a may dynamically modify the error detection sub-modules 315 and the error correction sub-modules 320 assigned to sectors 305 of flash memory 110-a. The controller 120-a may selectively power-up one or more of the error correction sub-modules 320 responsive to a monitored age or error rate associated with the flash memory 110-a. The controller 120-a may perform this monitoring on a per-sector basis, and the error correction sub-modules 320 may be powered-up to serve the sectors 305 where the error rates exceed a threshold. The controller 120-a may adapt the coding rate to be used by the encoder responsive to a monitored age or error rate associated with the flash memory 110-a. The controller 120-a may perform this monitoring on a per-sector basis, and the controller 120-a may adapt the coding rate on a per sector basis.

[0042] **FIG. 4** is a block diagram of a flash memory decoder system 400 illustrating certain controller functionality according to various embodiments of the invention. The system 400 includes an encoder 105-b, flash memory 110-b, a decoder115-b, and a controller 120-b. This system 400 may be an example of the system 100 of FIG. 1, and a component of this system 400 may have the same functionality as the counterpart component from FIG. 1 This flash memory system 400 may be a stand-alone device, or may be integrated (in whole or in part) with a computer, server, phone, mobile device, tablet, television, or any other computing device.

[0043] The controller 120-b includes an adaptive encoding rate controller 405, a power controller 410, a write controller 415, a read controller 420, an age monitoring module 425, and an error monitoring module 430. The age monitoring module 425 may monitor an age associated with the flash memory 110-b. This may be a time since manufacture, a time since first use, an amount of use, or any other metric which corresponds to the aging of the flash memory 110-b. This monitoring may involve direct monitoring of the flash memory 110-b itself, or may be based on reports from the encoder 105-b, decoder 115-b, or other components of the system.

[0044] The error monitoring module 430 may monitor an amount of errors associated with the flash memory 110-b. This monitoring may measure errors over a variety of time periods and metrics, and may be translated into an error rate. The monitoring may be performed on a per-sector (or per set of sectors) basis. A number of sampling and averaging techniques may be used. This monitoring may involve direct monitoring of the decoder 115-b itself, or may be based on reports from the decoder 115-b or other components of the system.

[0045] The adaptive encoding rate controller 405 may receive information on the rate and/or amount of errors from the error monitoring module 430. The adaptive encoding rate controller 405 may modify a coding rate to be used by the encoder 105-b when the monitored rate and/or amount of errors exceeds a threshold. The monitoring of errors may be performed on a per-sector, per set of sectors, or other regional basis. Thus, the coding rate to be used by the encoder 105-b may be modified when the monitored rate of errors for the applicable region exceeds a threshold. In some embodiments, the coding rate may be adapted to be more, or less, robust; in other embodiments, the adaptation is only to make the coding rate more robust. The adaptive encoding rate controller 405 may receive information on the age of the flash memory 110-b from the age monitoring module 425. The adaptive encoding rate controller 405 may adapt the coding rate based on this monitoring (e.g., implementing a more robust coding rate for one or more sectors of the flash memory 110-b when the age exceeds a threshold). There may be a number of different coding rate change thresholds related both to age and error rate. Moreover, these threshold may be adaptive to the amount of flash memory 110-b that remains available (e.g., the margin may be increased when the flash memory is utilized below a threshold amount).

[0046] As noted above, an decoder module 115 may include a number of error correction sub-modules. The power controller 410 may receive information on the age of the flash memory 100-b from the age monitoring module 425. The power controller 410 may selectively power-up (or power-down) one or more of the error correction sub-modules

responsive to an age of the flash memory 110-b. The power controller 410 may receive information on the rate and/or amount of errors from the error monitoring module 430. The power controller 410 may power-up (or power-down) one or more of the error correction sub-modules (e.g., when the monitored rate and/or amount of errors exceeds a threshold). The monitoring of errors may be performed on a per-sector, per set of sectors, or other regional basis. Thus, the power-up or power-down may be specific to a particular error correction sub-module for a given region of flash memory 110-b.

[0047] The write controller 415 may change the sectors of flash memory 110-b to be written to. These changes may be made in response to information from the age monitoring module 425 and error monitoring module 430. The read controller 420 may dynamically change the components of the decoder 115-b to be used to read different sectors of flash memory 110-b (e.g., in FIG. 3, the assignments of the decoder sub-modules 310, error detection sub-modules 315, and error correction sub-modules 320 may be changed in response to code rate modifications, increased errors, or age).

[0048] **FIG. 5** is a flowchart illustrating a method 500 of decoding data from a flash memory according to various embodiments of the invention. The method 500 may, for example, be performed in whole or in part by the system 100, 300, or 400 of FIG. 1, 3, or 4 or, more specifically, by the decoder 115 of FIG. 1, 2, or 4.

[0049] At block 505, encoded data from a flash memory is received. At block 510, the received encoded data is processed to generate a number of data streams. The information for each data stream may be a wholly or partially decoded before being forwarded to respective error correction sub-modules. At block 515, at each of a number of error detection sub-modules operating in parallel, a different one of the data streams is processed. Each error detection sub-module is configured to: detect whether a portion of the respective received stream contains an error, and forward the portion of the respective received stream containing an error to an error correction module. At block 520, at the error correction module physically separate from the error detection sub-modules, the forwarded portions of the respective received streams containing an error are corrected.

[0050] **FIG. 6** is a flowchart illustrating a method of age responsive decoding of data from a flash memory according to various embodiments of the invention. The method 600 may, for example, be performed in whole or in part by the system 100, 300, or 400 of FIG. 1, 3, or 4. The method 600 may be an example of the method 500 of FIG. 5.

[0051] At block 605, an age of a flash memory is monitored. At block 610, the coding rate for data to be encoded and stored in the flash memory is modified responsive to a first age threshold of the flash memory. At block 615, data is encoded at the modified rate, and the encoded data is stored on the flash memory. At block 620, one or more error correction sub-modules of an error correction module are powered-up from an inactive mode responsive to a second age threshold of the flash memory.

[0052] At block 625, the encoded data from the flash memory is processed to generate a number of partially decoded data streams. At block 630, at each of a number of error detection sub-modules operating in parallel, a different one of the data streams is processed. At block 635, a determination is made at each error detection sub-module whether a portion of the respective received stream contains an error. At block 640, error detection sub-modules forward those portions of the respective streams containing an error to the error correction module physically separate from the error detection sub-modules. At block 645, the error-free portions are forwarded to bypass the error correction module. At block 650, the portions of the respective received streams containing an error are corrected with the powered-up error correction modules and additional error correction modules.

[0053] **FIG. 7** is a flowchart illustrating a method of decoding data from a flash memory responsive to error rate according to various embodiments of the invention. The method 700 may, for example, be performed in whole or in part by the system 100, 300, or 400 of FIG. 1, 3, or 4. The method 700 may be an example of the method 500 of FIG. 5 or the method 600 of FIG. 6.

[0054] At block 705, a rate of errors from an error detection module is monitored for each of a number of sectors of the flash memory. At block 710, the coding rate for data to be encoded and stored in one or more sectors is modified responsive to the monitoring of first error rate threshold for the one or more sectors. At block 715, data is encoded at the modified rate and stored in the one or more sectors.

[0055] At block 720, an error correction sub-module assigned to the one or more sectors are powered-up from an inactive mode responsive to the monitoring of a second error rate threshold for the one or more sectors. At block 725, the encoded data from the one or more sectors is decoded to generate a decoded data stream. At block 730, at one of a number of error detection sub-modules operating in parallel, the decoded data stream is processed. At block 735, a determination is made by the error detection sub-module that a portion of the respective received stream contains an error. At block 740, the portion of the received stream

containing an error is forwarded to the powered-up error correction sub-module. At block 745, the forwarded portion is corrected with the powered-up error correction sub-module.

[0056] It should be noted that the methods, systems, and devices discussed above are intended merely to be examples. It must be stressed that various embodiments may omit, substitute, or add various procedures or components as appropriate. For instance, it should be appreciated that, in alternative embodiments, the methods may be performed in an order different from that described, and that various steps may be added, omitted, or combined. Also, features described with respect to certain embodiments may be combined in various other embodiments. Different aspects and elements of the embodiments may be combined in a similar manner. Also, it should be emphasized that technology evolves and, thus, many of the elements are examples and should not be interpreted to limit the scope of the invention.

[0057] Specific details are given in the description to provide a thorough understanding of the embodiments. However, it will be understood by one of ordinary skill in the art that the embodiments may be practiced without these specific details. For example, well-known circuits, processes, algorithms, structures, and techniques have been shown without unnecessary detail in order to avoid obscuring the embodiments.

[0058] Also, it is noted that the embodiments may be described as a process which is depicted as a flow diagram or block diagram. Although each may describe the operations as a sequential process, many of the operations can be performed in parallel or concurrently. In addition, the order of the operations may be rearranged. A process may have additional steps not included in the figure.

[0059] Moreover, as disclosed herein, the term "memory" or "memory unit" may represent one or more devices for storing data, including read-only memory (ROM), random access memory (RAM), magnetic RAM, core memory, magnetic disk storage mediums, optical storage mediums, flash memory devices, or other computer-readable mediums for storing information. The term "computer-readable medium" includes, but is not limited to, portable or fixed storage devices, optical storage devices, wireless channels, a sim card, other smart cards, and various other mediums capable of storing, containing, or carrying instructions or data.

[0060] Furthermore, embodiments may be implemented by hardware, software, firmware, middleware, microcode, hardware description languages, or any combination thereof. When implemented in software, firmware, middleware, or microcode, the program code or code

segments to perform the necessary tasks may be stored in a computer-readable medium such as a storage medium. Processors may perform the necessary tasks.

[0061] Having described several embodiments, it will be recognized by those of skill in the art that various modifications, alternative constructions, and equivalents may be used without departing from the spirit of the invention. For example, the above elements may merely be a component of a larger system, wherein other rules may take precedence over or otherwise modify the application of the invention. Also, a number of steps may be undertaken before, during, or after the above elements are considered. Accordingly, the above description should not be taken as limiting the scope of the invention.

WHAT IS CLAIMED IS:

1. A flash memory decoder comprising:

a decoding module configured to:

receive encoded data from the flash memory; and

decode the received encoded data to generate a plurality of partially decoded data streams;

an error detection module communicatively coupled with the decoding module, and comprising a plurality of error detection sub-modules operating in parallel, each error detection sub-module configured to:

receive a different one of the plurality of partially decoded data streams;

detect whether a portion of the respective received stream contains an error; and

forward the portion of the respective received stream containing an error to an error correction module; and

an error correction module, communicatively coupled with and physically separate from the error detection module, and configured to correct the received portions of the respective received streams containing an error.

2. The flash memory decoder of claim 1, wherein each of the error detection sub-modules is configured to read data from a set of one or sectors of flash memory different from other of the error detection sub-modules.

3. The flash memory decoder of claim 2, further comprising a read controller configured to dynamically modify the error detection sub-modules assigned to at least a subset of the sectors of flash memory.

4. The flash memory decoder of claim 1, wherein the error correction module comprises a plurality of error correction sub-modules operating in parallel and fewer in number than the error detection sub-modules.

5. The flash memory decoder of claim 4, further comprising a power controller configured to selectively power-up one or more of the error correction sub-modules responsive to an age of the flash memory.

6. The flash memory decoder of claim 4, further comprising:

an error monitoring module, communicatively coupled with the error detection module, and configured to monitor a rate of errors from the error detection module,

wherein the power controller is configured to selectively power-up one or more of the error correction sub-modules when the monitored rate of errors exceeds a threshold.

7. The flash memory decoder of claim 4, further comprising:

an error monitoring module, communicatively coupled with the error detection module, and configured to monitor a rate of errors from the error detection module for each of a plurality of sectors of the flash memory,

wherein a power controller is configured to selectively power-up an error correction sub-module for assignment to a set of one or more of the monitored sectors when the monitored rate of errors for the set exceeds a threshold.

8. The flash memory decoder of claim 4, wherein,

each error correction sub-module is assigned a set of two or more error detection sub-modules different from error detection sub-modules associated with other of the error correction sub-modules; and

each error correction sub-module is configured to receive portions of the respective received streams containing an error detected in parallel by the set of two or more error detection sub-modules assigned to the respective error correction sub-module.

9. The flash memory decoder of claim 1, further comprising a read controller configured to selectively power-down one or more subsets of the error detection sub-modules.

10. The flash memory decoder of claim 1, further comprising:

the flash memory, communicatively coupled with the decoding module;

an encoder, communicatively coupled with the flash memory, and configured to encode data at a coding rate for storage as the encoded data on the flash memory; and

an adaptive encoding rate controller configured to modify the coding rate responsive to an age of the flash memory.

11. The flash memory decoder of claim 1, further comprising:

an error monitoring module, communicatively coupled with the error detection module, and configured to monitor a rate of errors from the error detection module; and

an adaptive encoding rate controller configured to modify a coding rate for a flash memory encoding module when the monitored rate of errors exceeds a threshold.

12. The flash memory decoder of claim 1, further comprising:

an error monitoring module, communicatively coupled with the error detection module, and configured to monitor a rate of errors from the error detection module for each of a plurality of sectors of the flash memory; and

an adaptive encoding rate controller configured to modify a coding rate of a set of one or more of the monitored sectors when the monitored rate of errors for the set exceeds a threshold.

13. The flash memory decoder of claim 1, wherein each error detection sub-module is configured to direct error-free portions of the respective received streams to bypass the error correction module.

14. The flash memory decoder of claim 1, wherein,

the error detection module comprises the decoding module; and

the encoded data is encoded with a Hamming code, a BCH code, a Turbo code, or a low-density parity check code.

15. A system comprising:

an encoder configured to encode data for storage on a flash memory;

the flash memory, communicatively coupled with the encoding module, and configured to store the encoded data; and

a decoder, communicatively coupled with the flash memory, and configured to:

retrieve the encoded data from flash memory to generate a plurality of data streams; and

process, at each of a plurality of error detection sub-modules of the decoder operating in parallel, a different one of the plurality of data streams, wherein each error detection sub-module is configured to:

detect whether a portion of the respective received stream contains an error; and

forward the portion of the respective received stream containing an error to an error correction module of the decoder; and

correct, with the error correction module physically separate from the error detection module, the forwarded portions of the respective received streams containing an error.

16. The system of claim 15, wherein the encoder is further configured to adaptively modify the coding rate responsive to an age of the flash memory or a rate of errors associated with the decoded data.

17. A method comprising:

receiving encoded data from a flash memory comprising a plurality of data streams;

processing, at each of a plurality of error detection sub-modules operating in parallel, a different one of the plurality of data streams, wherein each error detection sub-module is configured to:

detect whether a portion of the respective received stream contains an error; and

forward the portion of the respective received stream containing an error to an error correction module; and

correcting, with the error correction module physically separate from an error detection module, the forwarded portions of the respective received streams containing an error.

18. The method of claim 17, further comprising:

dynamically modifying the error detection sub-modules assigned to receive data from respective sectors of flash memory.

19. The method of claim 17, wherein the error correction module comprises a plurality of error correction sub-modules operating in parallel and fewer in number than the error detection sub-modules.

20. The method of claim 19, further comprising:

powering-up, from an inactive mode, one or more of the error correction sub-modules responsive to an age of the flash memory.

21. The method of claim 19, further comprising:

monitoring a rate of errors from the error detection module; and

powering-up one or more of the error correction sub-modules when the monitored rate of errors exceeds a threshold.

22. The method of claim 19, further comprising:

monitoring a rate of errors from the error detection module for each of a plurality of sectors of the flash memory; and

powering-up an error correction sub-module for assignment to a set of one or more of the monitored sectors when the monitored rate of errors for the set exceeds a threshold.

23. The method of claim 17, further comprising:

modifying a coding rate for data to be stored as the encoded data on the flash memory responsive to an age of the flash memory.

24. The method of claim 17, further comprising:

monitoring a rate of errors from the error detection module; and

modifying a coding rate for data to be stored as the encoded data on the flash memory when the monitored rate of errors exceeds a threshold.

25. The method of claim 17, further comprising:

monitoring a rate of errors from the error detection module for each of a plurality of sectors of the flash memory; and

modifying a coding rate for data to be stored as the encoded data on the flash memory when the monitored rate of errors for the set exceeds a threshold.